

# **Miniature embedded real-time image processor system for smart sensor systems**

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## **ABSTRACT**

Programs at Nova Biomimetics have led to the design and development of a set of miniature electronics to be used for the application of a wide variety of point- and area-type mathematical operations to be applied in real time to the digital data produced by a variety of real-time digital video camera systems. Nova is planning to market these electronics in partial satisfaction of Small Business Innovation Research (SBIR) Program dual-use commercialization requirements.

## **1. INTRODUCTION**

Numerous ongoing programs at Nova Biomimetics have identified the need to produce a miniature image and signal processor architecture that can mate with existing cameras and cameras under development. Many of the existing projects currently make use of the digital video interface defined by the line of SE-IR Corporation cameras; in fact, Nova Biomimetics has developed the next-generation DSP board for SE-IR, so it makes sense to offer a co-processor board that can be re-configured to apply processing operations that offer the "next level" of advanced processing over and above the more conventional spatial fixed pattern nonuniformity correction and arbitrary pixel revectoring/bad pixel replacement functions of the SE-IR DSP board. In addition, a video converter is also in late stage development by Nova that will produce a VGA output. This converter has been designed to seamlessly interface to SE-IR's camera electronics, Nova's DSP and image processor boards.

## 2. OVERVIEW OF THE MINIATURE EMBEDDED DSP AND IMAGE PROCESSOR

### 2.1 General Description

Figure 1 shows the relationship between the functional blocks of the camera and processor system. These blocks include the front end sensor and camera electronics, communication interface, NUC processor, real time image processor and video converter. The host PC communicates with each functional block in the system through a high speed USB 2.0 interface. The system has been designed to support physical reconfiguration of various system components including the addition of one or more image processors. This benefit allows additional computing and memory buffering resources to be applied to complex, real time image processing algorithm implementations. In addition, a processor-to-camera electronics signal interface provides a communication feedback loop. This feature allows the reconfiguration of the camera electronics and/or sensor by the image processor(s) for systems that require this type of dynamic control.

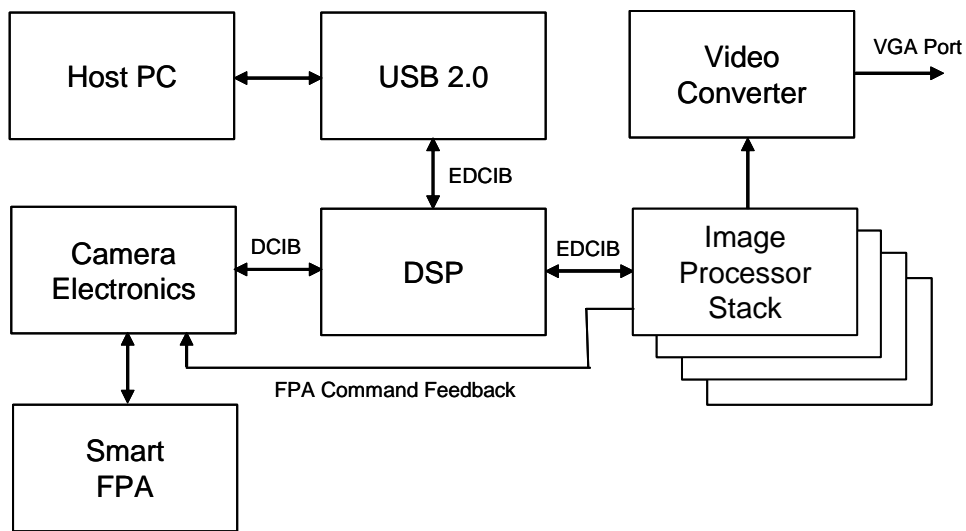


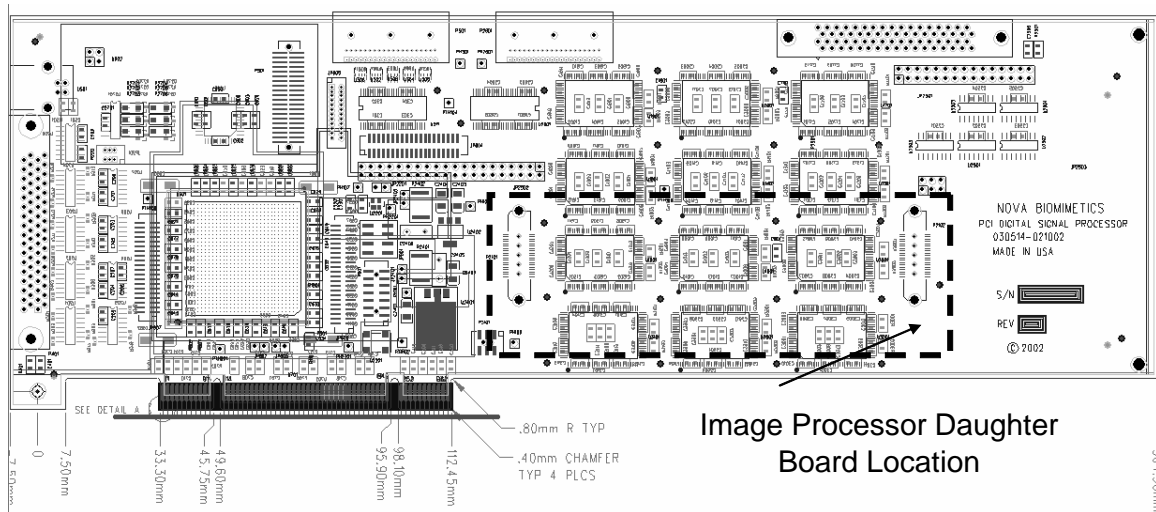
Figure 1: Smart Sensor Processor System Configuration

The following is a description of the miniature DSP and image processing blocks currently being developed at Nova Biomimetics:

- Compact, flexible unit
  - Fits in an existing compact chassis extrusion.
  - Flexible board stack, spacing.
  - High bandwidth interconnect thru RocketIO; no backplane required.
- Powerful image processing capabilities
  - DSB board optimized for NUC.
  - Image processor board; modular architecture can accommodate a wide variety of image and signal processing algorithms
  - Algorithms implemented with Xilinx et al IP, Matlab/Simulink, proprietary logic, and optional imbedded PowerPC software.
  - Image processor board includes over 1GB of RAM for image and data buffering.
- Modular, expandable architecture
  - RocketIO provides 1.6Gb/s full duplex IO between boards.
    - Images from one source can be passed to several boards for parallel processing.
    - Images/data can be passed from board-to-board for multi-stage processing.
    - Multiple source images can be passed to one board for combinatorial processing.
  - Parallel image IO allows multiple units to be interconnected to create a complex processing system.
- Nova IP or “Roll Your Own”
  - Nova has developed many innovative image processing algorithms, and can design custom firmware to customer specs.
  - Customers can optionally develop their own FPGA algorithms using the Xilinx tools and Nova-supplied system interface firmware (VHDL).

## 2.2 Application to SE-IR DSP Board

Nova has developed the next generation of SE-IR’s PCI form-factor Digital Signal Processor (DSP) card shown below in **Figure 2**. This board is currently in production. The DSP accepts 14 or 16 bit unsigned video and 12-bit signed or unsigned data. The DSP applies the requisite real-time spatial corrections to the video input received from the camera head assembly to compensate for focal plane array (FPA) fixed pattern nonuniformities. It also performs the function of arbitrary pixel revectoring and bad pixel replacement on video data rates up to 80 Mpixels/sec. DSP functions and camera configuration are controlled via the USB 2.0 communication interface from a host PC. This command and control is implemented using SE-IR’s “CamIRA” camera control and image acquisition software. The DSP has been designed to interface with an image processor card and/or video converter as shown in the figure.



**Figure 2:** Nova has developed the “next generation” PCI form-factor DSP board for SE-IR that offers processing expansion through the use of an “image processor daughterboard” interface.

Table 1 highlights the specifications of the PCI form factor DSP (DSP40). The PCI slot provides power and mechanical stability to the board. Bidirectional communication is provided through a USB 2.0 mezzanine card that plugs into the DSP board. The Enhanced Digital Command Interface Bus (EDCIB) communication protocol was developed by SE-IR Corporation and is used to communicate with the on-board FPGA. Board memory resources were sized to accommodate up to a 2-color 1024x768 format sensor input or over 1024x1024 format single color sensor input. Hooks have been incorporated into the design to accommodate larger format, multi-color sensor inputs as higher density memory become available.

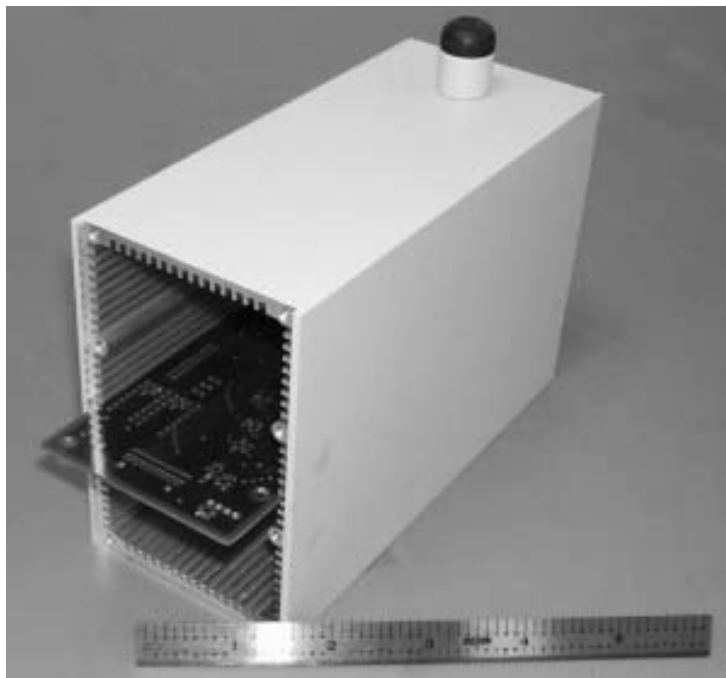
DSP40 Hardware Specification	
PWB Form Factor	PCI Standard Length Card: 312mm / 12.283"
Power Forms	PCI interface: 5.0 volts & 3.3 volts
Power Requirements	5.6W at 80 Mpixels/sec
Digital Input (12, 14 or 16 bits)	LVDS and TTL (selectable)
Digital Output	LVDS and TTL (selectable)
Pixel Rate	Up to 80 Mpixels/sec
Input Frame Format	1024x768 x 2-color
Control Interface	USB 2.0
Logic Resources	Xilinx FPGA: XC2V1000-5FF896C
Functions (selectable)	Spatial Nonuniformity
	Bad Pixel Replacement
	Pixel Revectoring
Image Processor Interface	EDCIB, NUC/bypass data and IP data

**Table 1: PCI form factor DSP specification.**

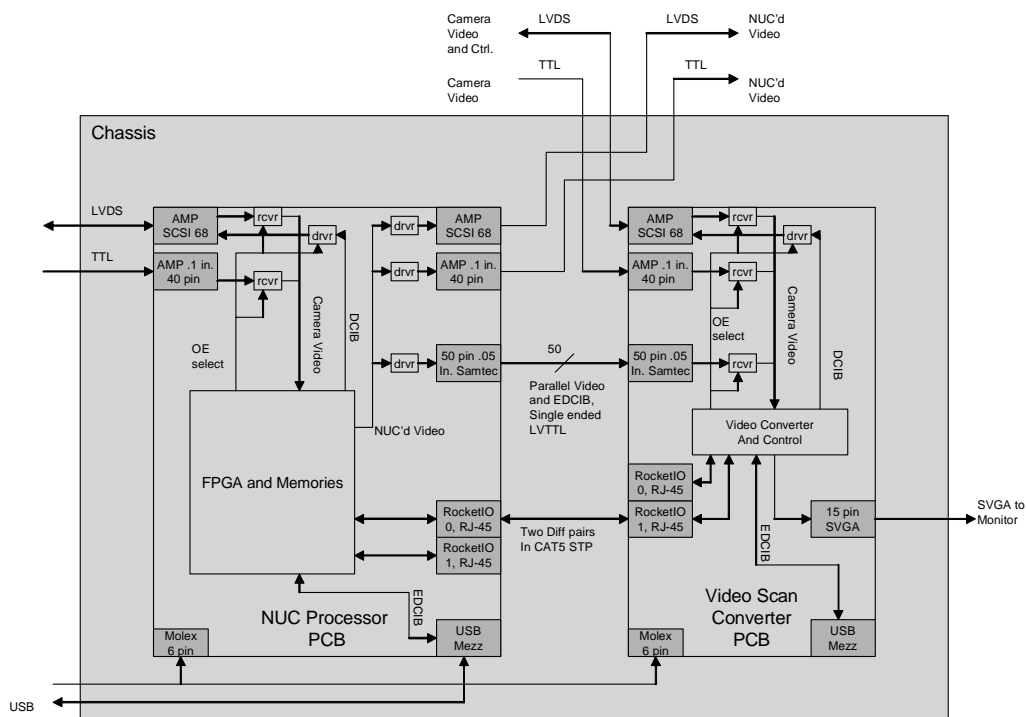
### 2.3 Application to SE-IR Small Camera Electronics

Nova has designed a more capable miniature version of the PCI form-factor DSP board. This smaller dual board set has been designed to fit within the standard SE-IR Small Camera enclosure as shown in Figure 3. This new board set retains all the functionality of the original PCI form-factor DSP design (refer to Figure 2.0) including NUC, bad pixel replacement and pixel revectoring operations. It also includes a high bandwidth data interface to communicate with down stream real-time image processors and/or video converters. Like the PCI form factor DSP, the mini DSP also supports pixel discrimination to the image processor and video converter when multi-color sensors are used in the system. This is important when applying color corrections and image fusion algorithms to the data.

Figure 4 shows the signal interconnects between the mini DSP and video converter. The video converter will produce a VGA output for real-time display of processed imagery. The same signal interface exists between the mini DSP and image processor boards. This common interface supports system expandability of additional image processor boards and video converters based on system requirements. Each processor block incorporates the RocketIO high speed communication interface to minimize IO bus count while maintaining high data throughput requirements. A LVTTTL interface has also been incorporated when the RocketIO interface is not required.



**Figure 3: Nova's small form-factor DSP and image processor board sets are being designed to fit within the SE-IR Small Camera system enclosure.**

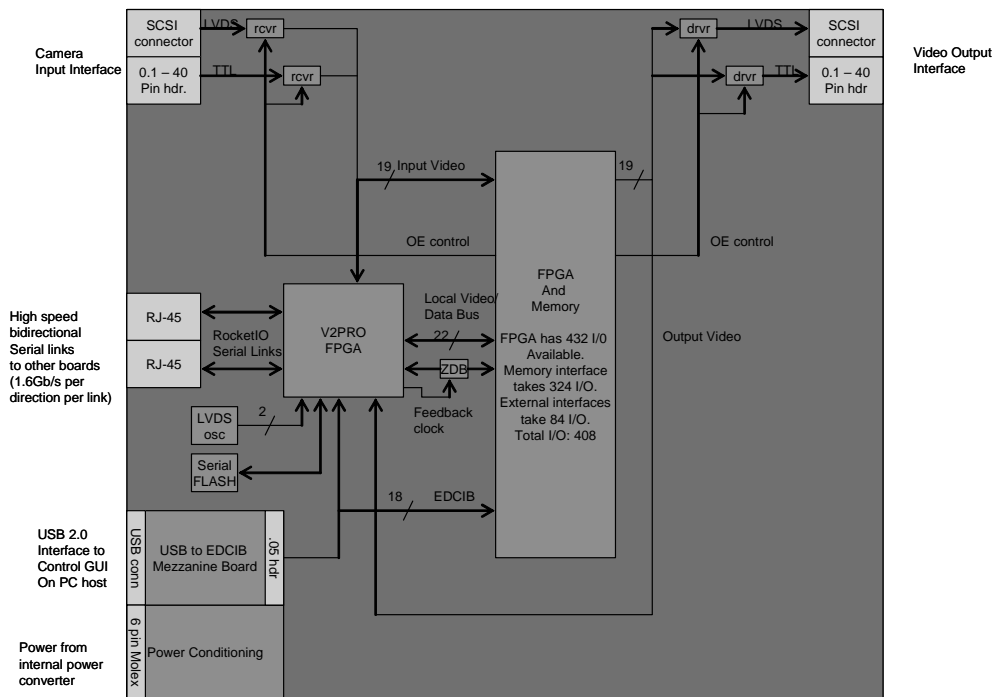


**Figure 4: Small Format DSP and Video Converter Unit Interconnect**

An image processor board set is being designed with a number of programmable large capacity FPGA devices and SRAM to support a hardware implementation of a wide variety of simple and complex processing algorithms performed in real time at data rates up to 80 Mpixels/second. Video data can be input directly to the image processor from the SE-IR camera electronics, the PCI form factor DSP or mini DSP board set.

So as to properly bound and partition the logic and memory requirements for each image processing board, a set of algorithms were evaluated. Some of these algorithms are discussed below. Depending upon the complexity of the algorithm, multiple boards may be stacked to partition the image processing operations into multiple parallel processing paths. In a stacked configuration, one of the processors will be used in a “master” configuration to direct the flow of data to individual “slave” FPGA devices and re-assembly of image data will be performed by a downstream processor. Figure 5 illustrates the image processor board concept.

These electronics enhance the computational power of the existing SE-IR camera system and satisfy operational requirements for numerous ongoing Nova Biomimetics technology development contracts. Nova will commercialize the resulting electronics in partial satisfaction of SBIR commercialization requirements.



**Figure 5: Small Format Image Processor Board Concept**

The following information describes current concepts regarding the implementation of this board set in a variety of form factors, as well as descriptions of algorithms that have already been committed to Xilinx designs in preparation for image processor hardware availability.

#### 2.4 Application to LEOIS2 Space-Qualifiable Hyperspectral Imaging Camera System

In a manner similar to how the image processor board set will serve as a co-processor to the SE-IR DSP board, a similar signal interface has been incorporated into the motherboard on the “Low Earth Orbiting Imaging Spectrometer” (LEOIS2) program at Nova Biomimetics. LEOIS2 is a Phase II SBIR for the AFRL/VSSS at Kirtland AFB, N.M. It makes use of a dual-color DRS 640 x 512 MCT LWIR FPA and a novel dual-octave spectrometer that is being produced by SSG Precision Optonics of Wilmington, MA. The LEOIS2 application requires the processor to perform the functions of dual-color spatial

nonuniformity correction as well as gain compensation for atmospheric and spectral effects. Figure 6 shows the LEOIS2 camera motherboard in the initial electronics testing phase. The figure shows the connector that is available for interfacing the image/signal processor to the motherboard. In the case of LEOIS2, the camera motherboard also incorporates a Virtex II FPGA processor as well as enough SRAM memory to perform a large number of real-time processing and image correction functions.

The Xilinx Virtex II family of devices has been chosen for the LEOIS2 application because of their inherent radiation tolerance. An on-board configuration PROM is used to reprogram the Virtex II device at power-up. The contents of the configuration PROM may be updated in the factory to permit a wide variety of processing functions to be available to the user.

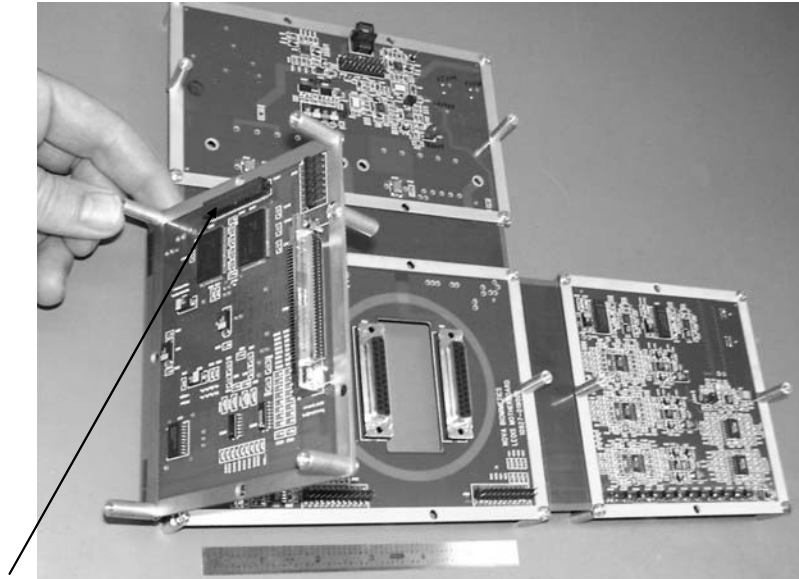


Image Processor Daughter  
Board Connector Location

**Figure 6: A version of the Image Processor board set will also be compatible with the LEOIS2 Camera Motherboard assembly. The mating connector to the processor board is shown.**

During the hardware design phase, Nova has invested substantial effort in developing a variety of real-time processing designs that will be ported to the Xilinx Virtex II family of devices. Some of these algorithms are specifically designed to modify the value of individual pixels; we refer to these as “point-applied” algorithms. A second class of algorithms exists in which the grey level values of numerous pixels are required in order to produce a processed representation for an individual pixel. We refer to these as “area-applied” algorithms. A discussion of these processing types follows as they have already been implemented in initial designs targeted for use in Nova’s image processor board system.

## 2.5 Point-Applied Algorithms

This class of mathematical processing operations modifies a single pixel’s value based on data stored in memory. The pixel’s value does not depend on values of surrounding or neighboring pixels. Virtex II point-applied processing designs have been produced at Nova for a variety of applications as described below.

### 2.5.1 *One- and Two-Point Nonuniformity Correction*

Infrared FPAs typically exhibit noticeable fixed-pattern spatial nonuniformities, the sources for which are related to nonuniformities in the CMOS fabrication process and variations between the gain and offset characteristics of amplifiers within individual unit cells or columns within the imager. Pure offset correction may be performed such that all pixels in the imager produce the same signal level at a specific incident flux level. When the illumination condition changes, though, if gain nonuniformities exist in the pixel distribution, fixed pattern spatial nonuniformities will again appear. For this reason, “two point” nonuniformity correction is typically performed such that, assuming linear behavior of all pixels over a specified flux range, all pixels will exhibit the same signal swing response. Nova has adopted SE-IR’s technique for applying such nonuniformity corrections and has developed the requisite Virtex II designs to accomplish these operations.

### 2.5.2 *Arbitrary Pixel Revectoring*

In order to keep the effective frame rate of a large pixel-count imager high, FPA manufacturers will typically multiplex parallel channels of data from the device. It is the job of a following processor to “shuffle” the parallel channels of data together to re-assemble a properly-displayed image. This function allows for the arbitrary spatial re-mapping of these pixel values by accessing re-vector address memory that stores the appropriate re-vectored locations.

### 2.5.3 *Bad Pixel Replacement*

Those pixels determined to be “bad” due to high temporal noise, low responsivity, etc. must be replaced by a spatial neighbor such that a “nice looking picture” is produced by the system. This is a form of arbitrary pixel revectoring in which the pre-computed pixel replacement map is accessed and the appropriate pixel grey level is provided from the camera system for subsequent display.

### 2.5.4 *Spectral Attenuation Compensation*

This function has been developed for the LEOIS2 program. Signal variations due to the selective absorption of radiant energy as a function of wavelength across the spectral range of the hyperspectral sensor may be compensated using this processing function. Pre-computed gain corrections are stored in SRAM and are clocked out of memory to be applied synchronously with the pixel data stream.

### 2.5.5 *Atmospheric Attenuation Compensation*

In a similar manner as that described above, a separate address range in memory may be programmed with atmospheric attenuation data and applied as gain corrections to all pixels in the imager. This assumes that the imager is using a wideband spectral incidence and that the compensated atmospheric attenuation applies to all pixels in the system.

### 2.5.6 *Pixel-based Mean and Standard Deviation Computation*

Automatic gain control algorithms require the knowledge of the real-time pixel value mean and standard deviation for control of the output display range through the use of lookup tables or other techniques. In addition, the spatial and temporal image noise contributions may be assessed through knowledge of the standard deviation metric. Nova designers have implemented West’s algorithm in Virtex II firmware designs to produce frame-based measurements for both the frame mean and standard deviation. This information is made available to the FPGA for other functions required of the processing system.

### 2.5.7 Real-time pixel-based FFT and PSD Computation

Nova is in the process of investigating the use of “hyper-temporal” processing algorithms to evaluate the temporal signatures of objects that emit modulated IR energy in the audio regime. Fast-running FFT operations have been implemented in Virtex II firmware for this purpose. This information has been used to perform real-time evaluations of power spectral densities (PSDs) for each pixel in the imager, followed by conditional tests to attempt to “find” single-pixel objects with such temporal signatures.

### 2.5.8 Tag Bits

As with the LEOIS2 system that uses a dual-color FPA, other applications will arise where the user would like to keep track of pixels with individual characteristics (e.g., color band). The camera systems in typical use today (including those produced by SE-IR) make use of 14-bit video data and the processing bus widths on the processor board are wide (in some cases > 40 or 50 bits) in order to maintain computational precision. “Tag bits” produced by the camera head or stored in memory on the DSP board are carried through the processing chain such that at a later time these pixel values may be “discriminated” from each other.

## 2.6 Area-Applied Algorithms

A second major group of processing functions makes use of pixel values that are spatially distributed around the “pixel of interest”. These operations make use of the spatial relationships between pixels in order to produce a final processed value. Many such algorithms exist and the ones described below are those that have been implemented in Virtex II firmware in preparation for hosting by Nova’s image processor.

### 2.6.1 Convolution Processing

A wide variety of image processing operations may be performed using conventional convolution processing in which a spatial “kernel” is used to define the particular processing operation. The kernel’s values are convolved with the pixel grey level values to produce a single value for the “pixel of interest” that is written to the output image. Convolution processing is accomplished by accessing the kernel data stored in memory and successively producing convolved results with the input data, writing to an output buffer in a rasterized order throughout the image.

Many types of image processing operations may be performed using convolution processing including (but not limited to) blurring, averaging, spatial noise reduction, unsharp masking, Difference of Gaussian filtering, Laplacian of the Gaussian filtering, selective motion detection, edge enhancement and many others.

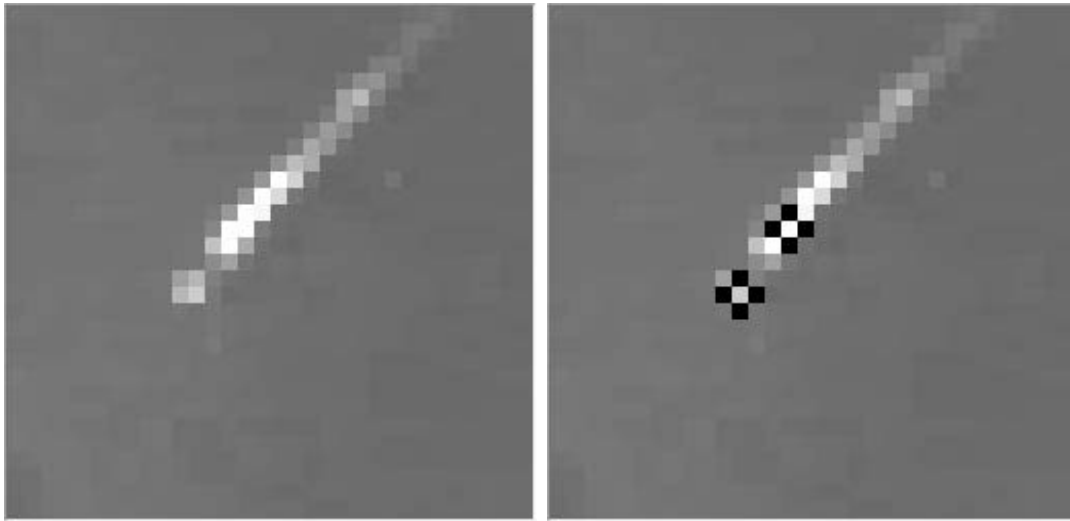
### 2.6.2 Area-Weighted Centroid Target Tracking

As part of Nova’s ongoing work on AFRL and MDA SBIR projects, we have developed an area-weighted centroid target tracking algorithm based on the use of Xilinx Virtex II FPGA devices. The existing technique has the capability of tracking up to four independent targets, reporting their individual area centroids and suggesting the spatial extent of the target within the field of view. This is important for application to real-time use of the “Variable Acuity Superpixel Imaging” (VASI) devices that we have developed for high-speed, high-resolution, wide field-of-view imaging applications<sup>1</sup>.

Figure 7 shows an example output from the Virtex II code in which it has identified two distinct targets and identified their locations as indicated in the right panel. This is an actual sequence of MWIR imagery from a boosting target that has just undergone second-stage separation and the second stage, moving downrange, is beginning to separate from the boost vehicle.

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<sup>1</sup> Curzan, J.P., C. R. Baxter and M. A. Massie, “Variable Acuity Imager with Dynamically Steerable, Programmable Superpixels”, SPIE Aerosense Infrared Technology and Applications XXVIII, Seattle, WA., 2002.

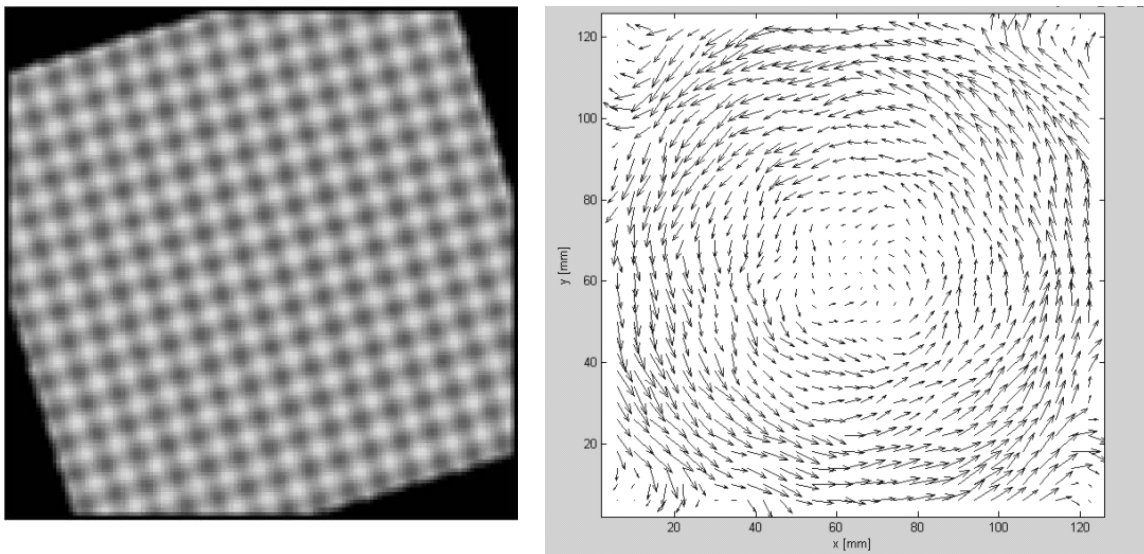


**Figure 7: Up to four objects may be tracked using Nova’s area-weighted multiple target tracking algorithm.**

### 2.6.3 Optical Flow Vector Field Computation

Other applications exist which require a real-time estimation of the image velocity flow field. This may be applied to sensor egomotion sensing, target/object identification and tracking against a moving background. In addition, these techniques can be used to compute focus of expansion, time to contact and many other motion properties of images that can be used to control robots, for example. Tracking systems can use the extracted velocity information; segmentation of moving objects can be realized by using the detection of motion discontinuities<sup>2</sup>. Using optical flow fields, spatial clutter may be reduced by eliminating pixel responses moving in specified directions.

A “first-cut” Virtex II design for an optical flow computation engine based on principals developed by Horn and Schunk<sup>3</sup> has been designed with a representative vector flow field shown in Figure 8. Our design is progressing and we expect to be able to apply it to a variety of real-world problems.



**Figure 8: Optical flow field properties of image data may be computed using Nova’s evolving Virtex II-based design.**

<sup>2</sup> Mehta, Swati and Ralph Etienne-Cummings, “Normal Optical Flow Chip”, ISCAS 2003, Bangkok, Thailand.

<sup>3</sup> Horn, B. K. and Schunk, B.G., “Determining Optical Flow”, Artificial Intelligence, 1981, Vol. 17, pp. 185 – 203.

#### 2.6.4 Variable Acuity Superpixel Imager (VASI) Image Reconstruction

Nova Biomimetics has developed a novel two-dimensional imaging chip whose design is based on properties exhibited by biological retinas. The “Variable Acuity” imager permits the user to program a unique spatial arrangement of “superpixels” that may be updated in real time. In effect, any spatial configuration of pixels in the imager may be realized by programming the device in a way that permits pixels to share their individually-collected photocharge with any or all of their neighbors. Single and multiple “foveal” configurations are possible, and these high spatial resolution regions may be “flown” around the FPA at the will of the controlling processor at the frame rate.

This device was developed through the combined requirements of (a) covering a wide total field of view while (b) retaining the highest possible spatial resolution on the targets of interest while at the same time (c) operating at the highest possible frame rate. Many thousands of frames per second are possible with the prototype imager while maintaining high spatial resolution.

Based upon technology developments produced over the last decade, it is now possible to design a focal plane array (FPA) that incorporates a dynamic, user-defined spatial distribution of pixels. Although virtually any spatial configuration (i.e., size and location) of pixels could be defined, an important first system that has been realized has been programmed to represent the spatial configuration of the vertebrate fovea.

A “foveal FPA” as discussed here has the property of higher spatial frequency of pixel channels near the “center of attention” (COA), with a radially-symmetric spatial frequency diminishing radially out from the COA. The device as described permits the user to define any desired spatial distribution of pixels, and may change this distribution at the frame rate, if desired. In this way, the COA may be directed to move within the total field of view of the FPA in order to track objects of interest with high angular precision, without sacrificing the ability to detect other potential targets which may enter into the sensor’s periphery.

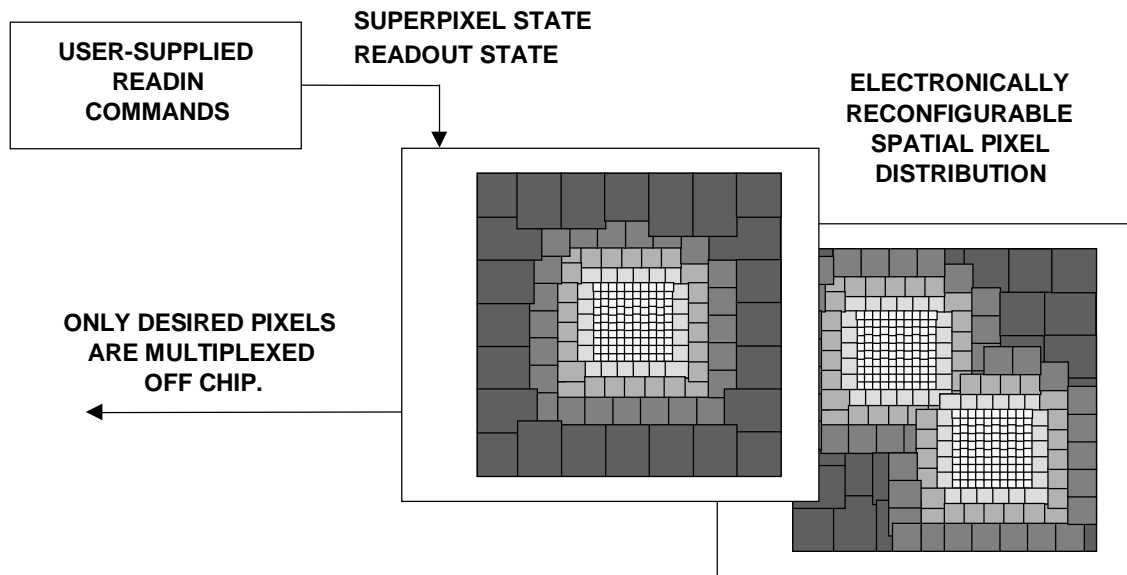
The basic operational properties of the visible and infrared VASI devices that have been developed are:

- User-defined spatial distribution of pixels permits high accuracy “on target”, while retaining detection over the entire field-of-view (FOV). Each pixel gets programmed into a specific “superpixel” state, and it will “know” how to share its charge with neighbors such that a resulting superpixel distribution is produced.
- High frame rates are possible by programming the device into a superpixel state; pixels (whether they are “standard pixels” or “superpixels”) need to deliver only one analog data value per frame. This will minimize the total number of pixel values required to be delivered off-FPA, thus maximizing effective frame rate.

Figure 9 demonstrates the concept of “FPA READIN Programmability”, resulting in a user-defined effective distribution of pixels. Also indicated in the figure is that the readout state for each pixel may be programmed individually through the use of the READIN command.

High frame rate is achieved by only multiplexing out pixel values from individual superpixels and not each and every “standard” pixel on the FPA. The FPA sends out the analog pixel value for each superpixel; in addition, if commanded, it can report its current spatial configuration state such that a normal 2D image representation may be reconstructed for human viewing applications.

A Virtex II algorithm has been designed and tested that performs the 2D image reconstruction operation for use with VASI sensors. This is a critical initial processing step required when using VASI sensors if algorithms must be applied to the VASI data that are based on spatial relationships between neighboring pixels. Virtually all convolution-based operations must use such a pre-processing reconstruction step before they may be applied to the real-time data.



**Figure 9: High-speed compressed image data is produced by Nova’s family of VASI sensors because only a single pixel value is multiplexed out of any individual superpixel. A Virtex II algorithm was produced that reconstructs the compressed data.**

### 2.6.5 Rank Filters

Rank filters are area-type processing operations that further require the collected pixel-based values to be sorted or combined in some manner as a means to select which value is passed on to the output of the process. Local adaptive filters have proved their advantages in image processing for edge-preserved image denoising and deblurring, image segmentation, and reliable object detection.

#### 2.6.5.1 Median Filter

One type of rank filter that has been implemented in Virtex II firmware at Nova is the linear median filter. This filter makes use of a user-specified even number of pixel values on either side of a central pixel (in its same row), sorts the collection of values and selects the value that is directly in the center of the distribution of values. This is the value that is passed to the output.

Such a filter is very effective in reducing or eliminating “salt and pepper” noise in data values (i.e., it improves data monotonicity in the presence of noise). We have implemented such a filter in the “background velocimetry” and “hypertemporal signal detection” work as previously described to reduce the effect of noise.

Nova designers have also developed a 2D median filter in Virtex II firmware. As the Nova Image Processor hardware is further developed, many more filtering types will be developed and available for customer use.

## 3. ACKNOWLEDGEMENTS

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